

New!



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71670 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71670 includes general purpose and gigabit serial connectors for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions,

a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

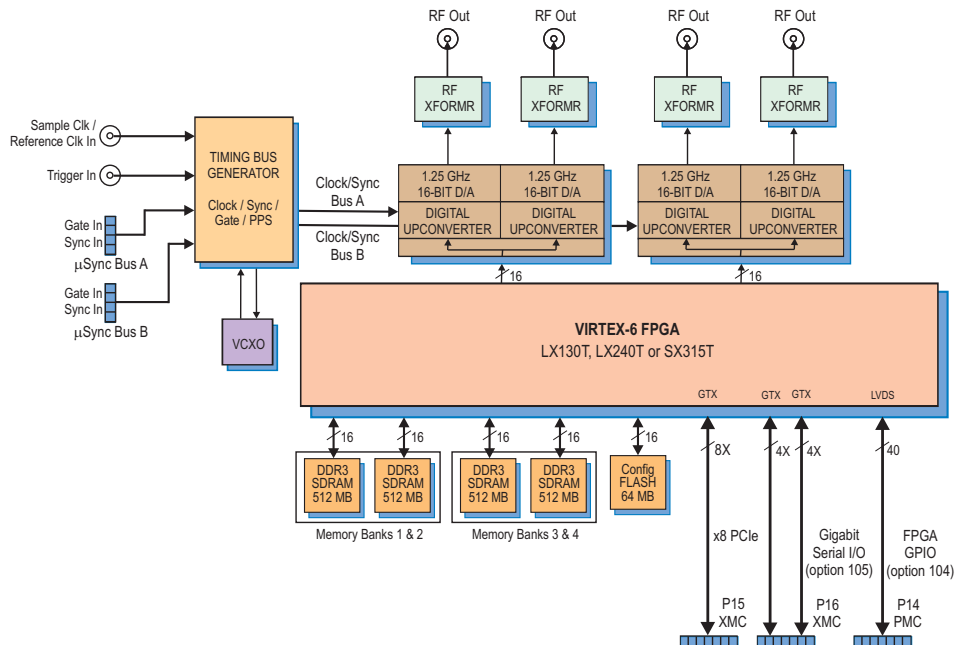
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ▶



► Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a base-band real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7192 or 9192 Cobalt Synchronizers can drive multiple 71670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 71670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

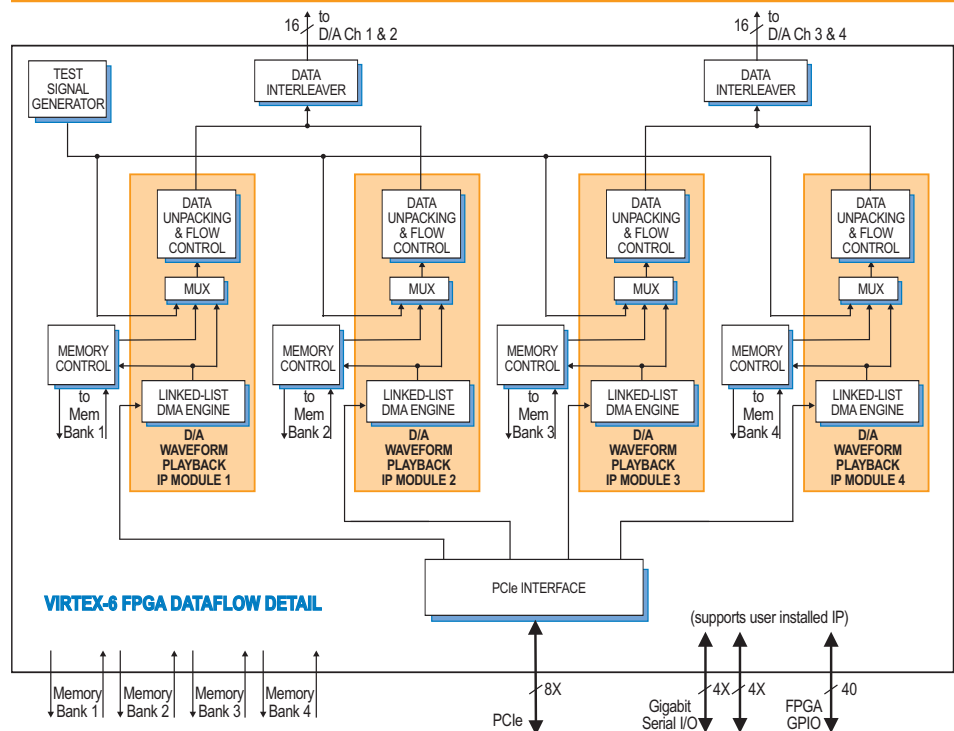
The Model 71670 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71670 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application. ►

D/A Waveform Playback IP Module

The Model 71670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



### Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

Model	Description
71670	4-Channel 1.25 GHz D/A with Virtex-6 FPGA - XMC

#### Options:

-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

\* These options are always required

*Contact Pentek for availability of rugged and conduction-cooled versions*

Model	Description
8266	PC Development System See 8266 Datasheet for Options

### ► PCI Express Interface

The Model 71670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

### Specifications

#### D/A Converters

**Type:** TI DAC3484  
**Input Data Rate:** 312.5 MHz max.  
**Output Bandwidth:** 250 MHz max.  
**Output Sampling Rate:** 1.25 GHz max. with interpolation  
**Interpolation:** 2x, 4x, 8x or 16x  
**Resolution:** 16 bits

#### Front Panel Analog Signal Outputs

**Quantity:** Four D/A outputs  
**Output Type:** Transformer-coupled, front panel female SSMC connectors  
**Full Scale Output:** Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps  
**Full Scale Output Programming:**  $1.0 \times (G+1) / 16$  Vp-p, where 4-bit integer  $G = 0$  to 15

#### Clock Synthesizer

**Clock Source:** Selectable from on-board programmable VCXO or front panel external clock  
**VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz  
**Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz  
**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

#### External Clock

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

#### External Trigger Input

**Type:** Front panel female SSMC connector  
**Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus:** 19-pin  $\mu$ Sync bus connector includes sync and gate/trigger inputs, CML

#### Field Programmable Gate Array

**Standard:** Xilinx Virtex-6 XC6VLX130T-2  
**Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

#### Custom I/O

**Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA  
**Option -105:** Installs the XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

**Memory:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

#### PCI-Express Interface

**PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

#### Environmental

**Operating Temp:** 0° to 50° C

**Storage Temp:** -20° to 90° C

**Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.