Model 56641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - AMC

General Information

Model 56641 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56641 includes a front panel general-purpose connector for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

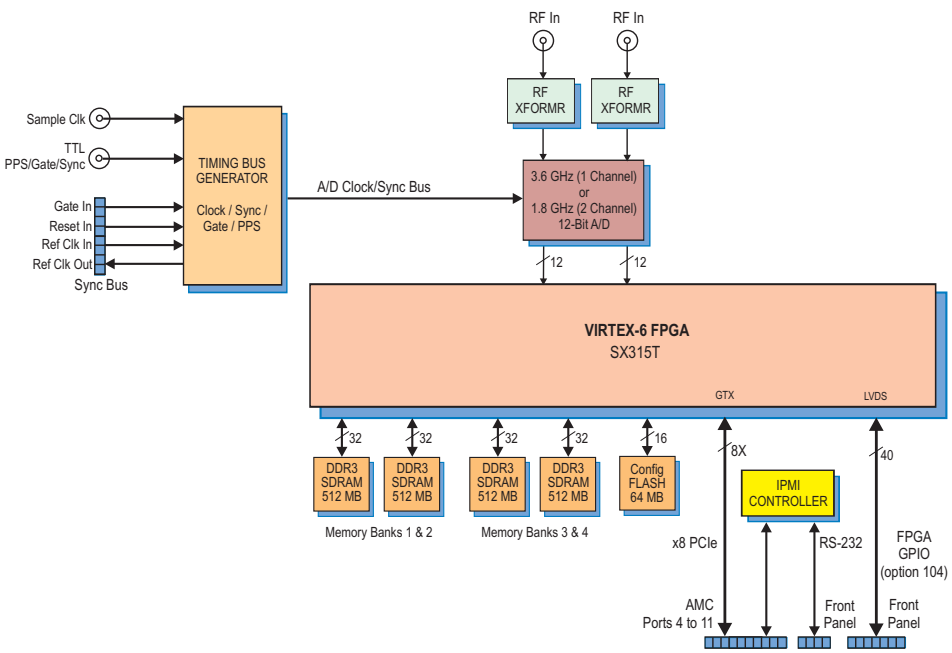
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

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A/D Acquisition IP Module

The 56641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

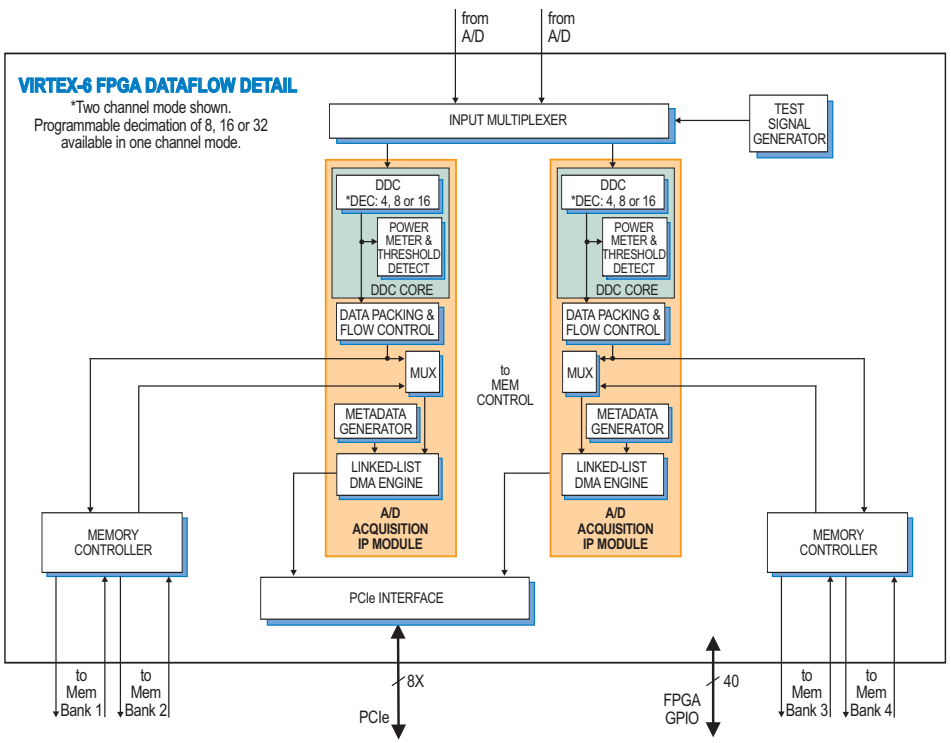
➤ Clocking and Synchronization

The 56641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The sync bus includes gate, reset, and in and out reference clock signals. Two 56641's can be synchronized with a simple cable. For larger systems, multiple 56641's can be synchronized using the Cobalt 7192 high-speed sync module to drive the sync bus.

Memory Resources

The 56641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
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➤ AMC Interface

The Model 56641 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin front panel connector, includes gate, reset, and in and out ref clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include trigger and gate

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-6 FPGA - AMC
Options:	
-002*	-2 FPGA speed grade
-064*	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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