

New!

# Model 56791

# L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - AMC



### Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multiboard synchronization
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

### General Information

Model 56791 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56791 includes general purpose and gigabit serial connectors for application-specific I/O.

### The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 56791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 56791 can operate as a complete turnkey solution with no need to develop FPGA IP.

### Extendable IP Design

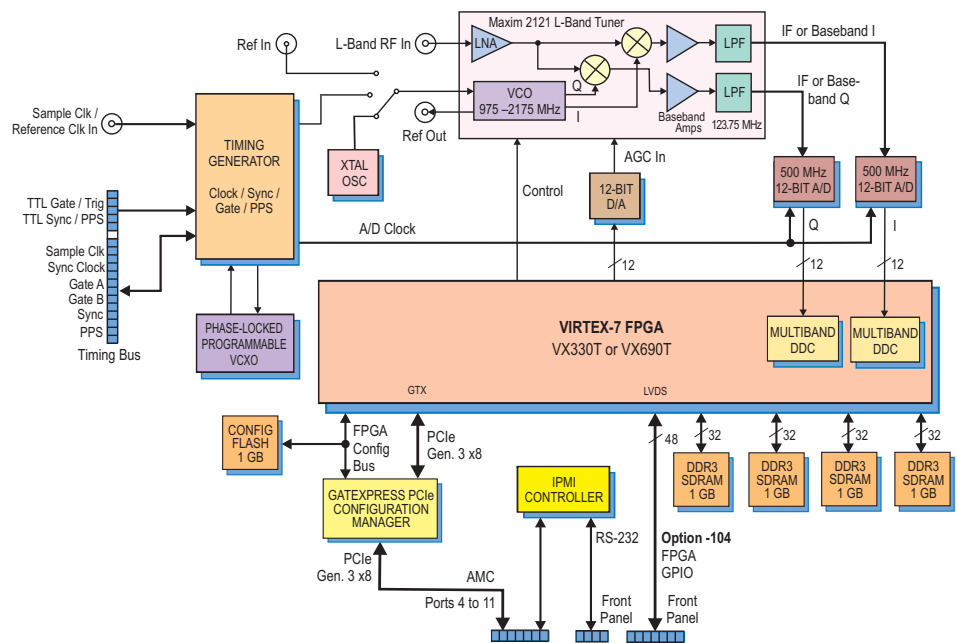
For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤



**A/D Acquisition IP Modules**

The 56791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8 \cdot f_s / N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

**RF Tuner Stage**

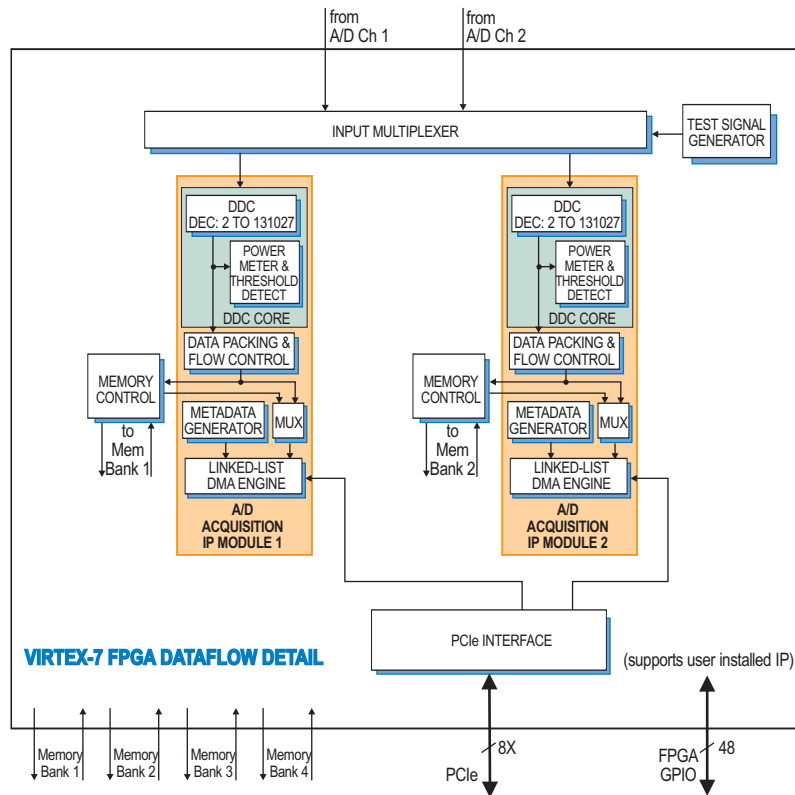
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from -50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each. ▶



► In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

### GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

### A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

### A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

### Memory Resources

The 56791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

### AMC Interface

The Model 56791 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or  $\mu$ TCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

### PCI Express Interface

The Model 56791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ►

### ► Specifications

#### Front Panel Analog Signal Input

**Connector:** Front panel female SSMC

**Impedance:** 50 ohms

#### L-Band Tuner

**Type:** Maxim MAX2121

**Input Frequency Range:** 925 MHz to 2175 MHz

**Monolithic VCO Phase Noise:**

-97 dBc/Hz at 10 kHz

**Fractional-N PLL Synthesizer:**

$\text{freq}_{\text{VCO}} = (\text{N.F.}) \times \text{freq}_{\text{REF}}$

where integer N = 19 to 251 and fractional F is a 20-bit binary value

**PLL Reference (freq<sub>REF</sub>):** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

**LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter

**Usable Full-Scale Input Range:**

-50 dBm to +10 dBm

**Baseband Low Pass Filter:**

3 dB cutoff frequency: 123.75 MHz

#### A/D Converters

**Type:** Texas Instruments ADS5463

**Sampling Rate:** 10 MHz to 500 MHz

**Resolution:** 12 bits

**Option -014:** 400 MHz, 14-bit A/Ds

**Sample Clock Sources:** On-board timing generator/synthesizer

#### A/D Clock Synthesizer

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

#### Timing Generator External Clock Input

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**Timing Generator Bus:** 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### External Trigger Input

**Quantity:** 2

**Type:** Front panel female SSMC connector, LVTTTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

#### Field Programmable Gate Array

**Standard:** Xilinx Virtex-7 XC7VX330T-2

**Optional:** Xilinx Virtex-7 XC7VX690T-2

#### Custom I/O

**Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

#### Memory

**Type:** DDR3 SDRAM

**Size:** Four banks, 1 GB each

**Speed:** 800 MHz (1600 MHz DDR)

#### PCI-Express Interface

**PCI Express Bus:** Gen. 1, 2 or 3\*: x4 or x8

#### Environmental

**Operating Temp:** 0° to 50° C

**Storage Temp:** -20° to 90° C

**Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.

## Ordering Information

Model	Description
56791	L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - AMC

#### Options:

-014	400 MHz, 14-bit A/Ds
-076	XC7VX690T-2 FPGA
-100	27 MHz crystal for MAX2121
-104	LVDS FPGA I/O through front-panel connector

Contact Pentek for availability of rugged versions

\* Gen 3 requires a compatible backplane and SBC