

New!

# Models 57760 & 58760

# 4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 6U OpenVPX



Model 58760



## General Information

Models 57760 and 58760 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a VPX carrier board.

Model 57760 is a 6U board with one Model 71760 module while the Model 58760 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

## The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchro-

nization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

## Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

## Xilinx Virtex-7 FPGA

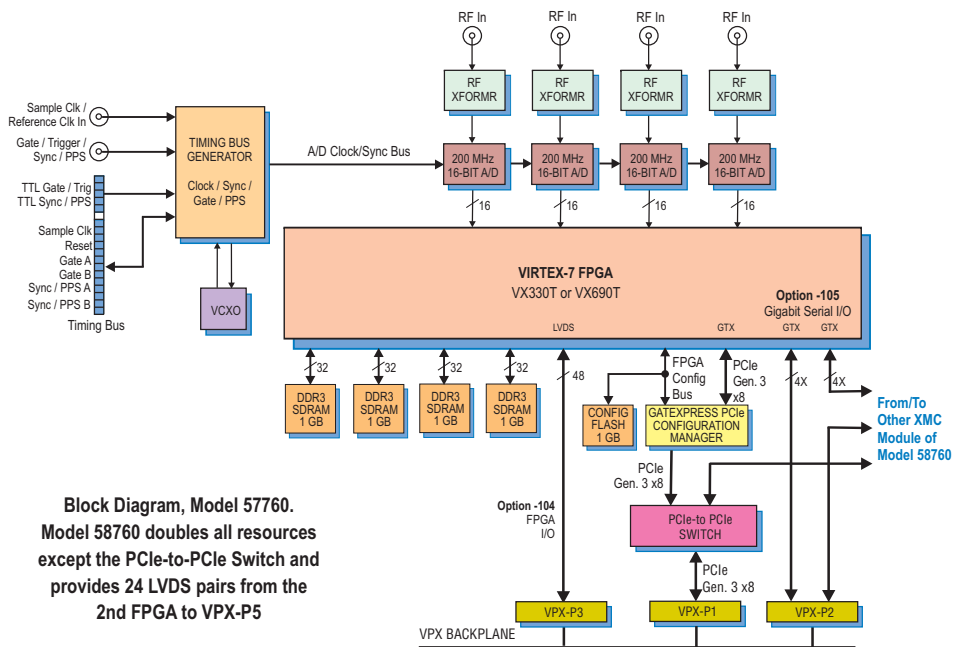
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760. ➤

## Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



► **GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvola-

tile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

**A/D Converter Stages**

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

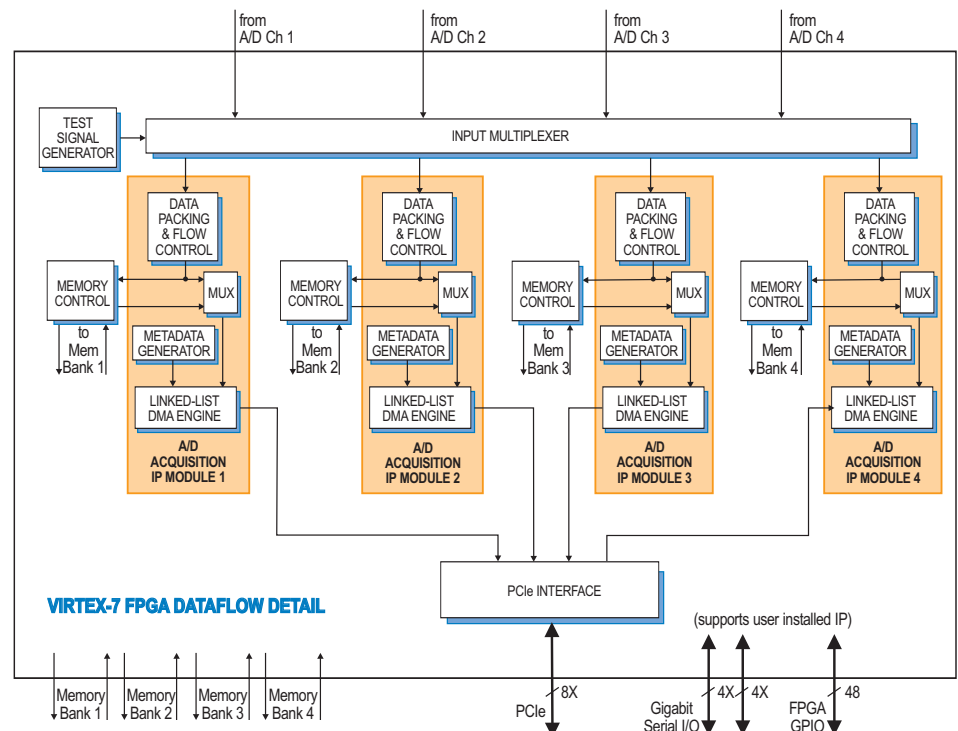
The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources. ►

**A/D Acquisition IP Modules**

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► **Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Model 57760: 4 A/Ds**

**Model 58760: 8 A/Ds**

**Front Panel Analog Signal Inputs (4 or 8)**

**Input Type:** Transformer-coupled, front panel female SSMC connectors

**Transformer Type:** Coil Craft WBC4-6TLB

**Full Scale Input:** +8 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters (4 or 8)**

**Type:** Texas Instruments ADS5485

**Sampling Rate:** 10 MHz to 200 MHz

**Resolution:** 16 bits

**Sample Clock Sources: (1 or 2)**

On-board clock synthesizer

**Clock Synthesizers (1 or 2)**

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clocks (1 or 2)**

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus (1 or 2)**

26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Inputs (1 or 2)**

**Type:** Front panel female SSMC connector, LVTTTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

**Standard:** Xilinx Virtex-7 XC7VX330T-2

**Optional:** Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**

**Option -104:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760

**Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760.

**Memory Banks (4 or 8)**

**Type:** DDR3 SDRAM

**Size:** 1 GB each

**Speed:** 800 MHz (1600 MHz DDR)

**PCI-Express Interface**

**PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental:** Level L1 & L2 air-cooled;

Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

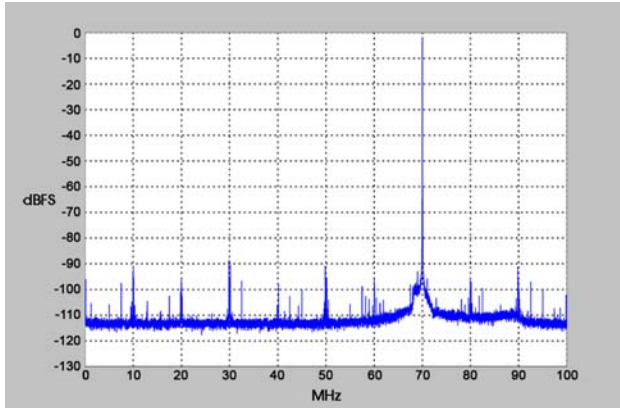
**Ordering Information**

Model	Description
57760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U VPX
58760	8-Channel 200 MHz 16-bit A/D with two Virtex-7 FPGAs - 6U VPX
<b>Options:</b>	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57760; P3 and P5 connectors, Model 58760
-105	Gigabit link between the FPGA and P2 connector, Model 57760; gigabit links from each FPGA to P2 connector, Model 78760

*Contact Pentek for availability of rugged and conduction-cooled versions*

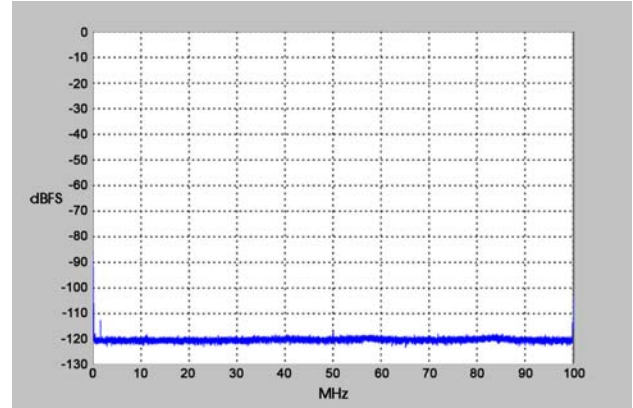
A/D Performance

Spurious Free Dynamic Range



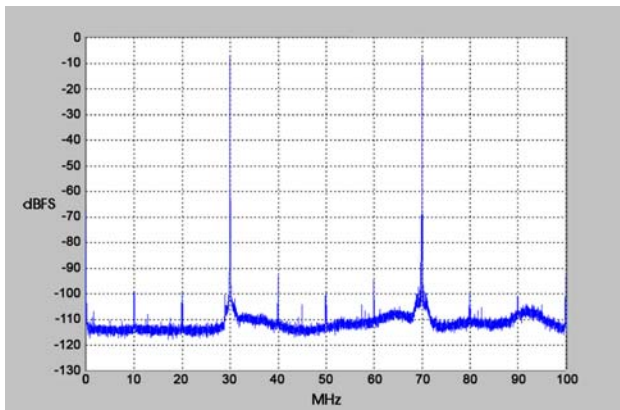
$f_{in} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Internal Clock

Spurious Pick-up



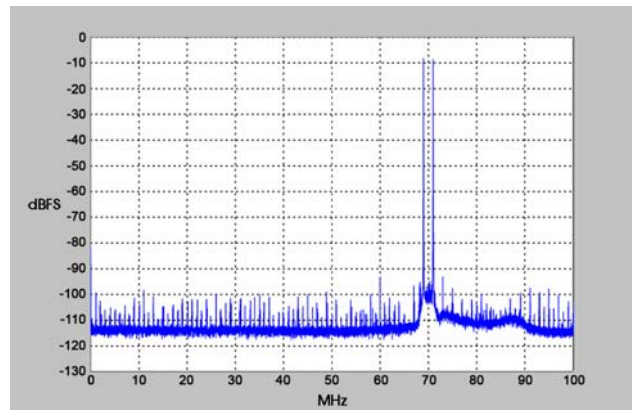
$f_s = 200 \text{ MHz}$ , Internal Clock

Two-Tone SFDR



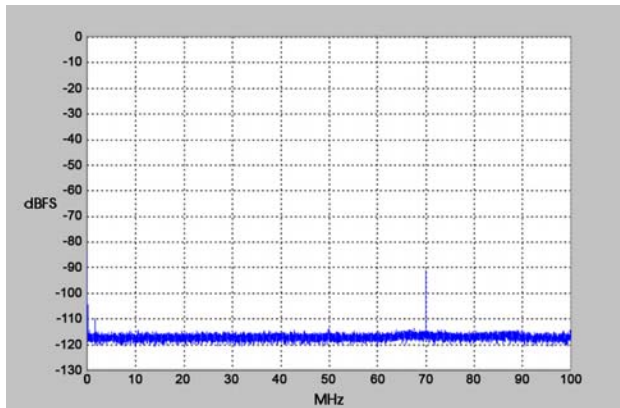
$f_1 = 30 \text{ MHz}$ ,  $f_2 = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

Two-Tone SFDR



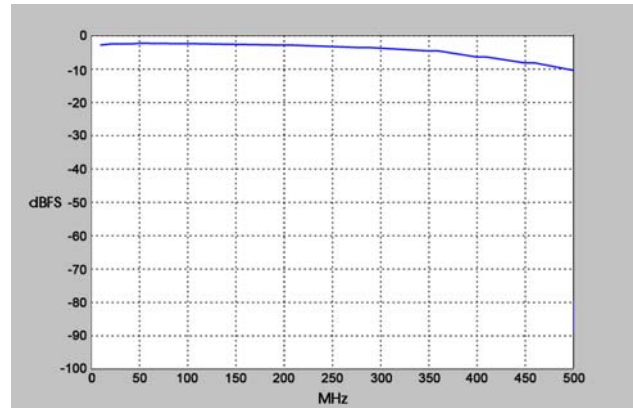
$f_1 = 69 \text{ MHz}$ ,  $f_2 = 71 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



$f_{in \text{ Ch2}} = 70 \text{ MHz}$ ,  $f_s = 200 \text{ MHz}$ , Ch 1 shown

Input Frequency Response



$f_s = 200 \text{ MHz}$ , Internal Clock